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(54) Compression circuitry for generating an encoded bitstream from a plurality of video frames

(57) Compression circuitry for generating an encoded bitstream from a plurality of video frames. Data is DCT transformed and then streamed to a processor where quantised and inverse quantised blocks are generated. A second streaming data connection streams the inverse quantised blocks to an inverse DCT block to generate reconstructed prediction error macroblocks. An addition circuit adds each reconstructed prediction error macroblock and its corresponding predictor macroblock to generate a respective reconstructed macroblock. The quantised macroblocks are zig-zag scanned, run level coded and variable length coded to generate an encoded bitstream.

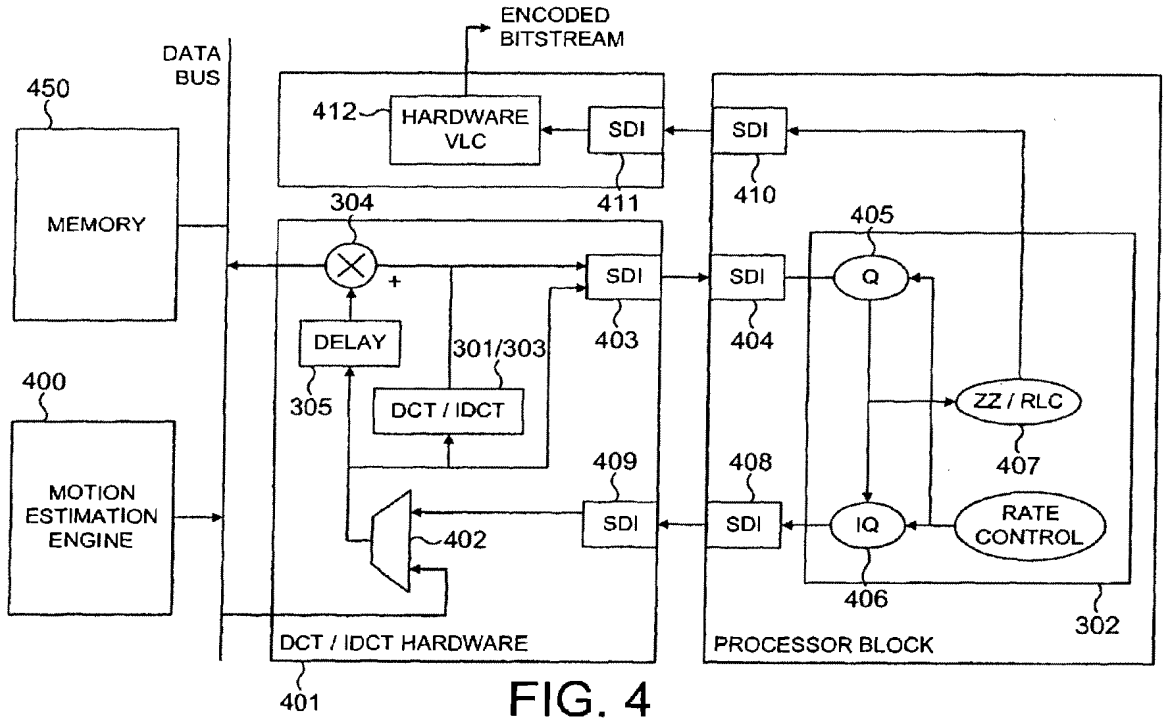

FIG. 4

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Description

FIELD OF INVENTION

[0001] The present invention relates to motion picture compression circuits for pictures such as television pictures, and more particularly to a compression circuit complying with H.261 and MPEG standards.

BACKGROUND OF THE INVENTION

[0002] Figures 1A-1C schematically illustrate three methods for compressing motion pictures in accordance with H.261 and MPEG standards. According to H.261 standards, pictures may be of intra or predicted type. According to MPEG standards, the pictures can also be of bidirectional type.

[0003] Intra ("I") pictures are not coded with reference to any other pictures. Predicted ("P") pictures are coded with reference to a past intra or past predicted picture. Bidirectional ("B") pictures are coded with reference to both a past picture and a following picture.

[0004] FIG. 1A illustrates the compression of an intra picture I1. Picture I1 is stored in a memory area M1 before being processed. The pictures have to be initially stored in a memory since they arrive line by line whereas they are processed square by square, the size of each square being generally 16.times.16 pixels. Thus, before starting to process picture I1, memory area M1 must be filled with at least 16 lines.

[0005] The pixels of a 16.times.16-pixel square are arranged in a so-called "macroblock". A macroblock includes four 8.times.8-pixel luminance blocks and two or four 8.times.8-pixel chrominance blocks. The processes hereinafter described are carried out by blocks of 8.times.8 pixels.

[0006] The blocks of each macroblock of picture I1 are submitted at 10 to a discrete cosine transform (DCT) followed at 11 by a quantisation. A DCT transforms a matrix of pixels (a block) into a matrix whose upper left corner coefficient tends to have a relatively high value. The other coefficients rapidly decrease as the position moves downwards to the right. Quantisation involves dividing the coefficients of the matrix so transformed, such that a large number of coefficients which are a distance away from the upper left corner are cancelled.

[0007] At 12, the quantified matrices are subject to zigzag scanning (ZZ) and to run/level coding (RLC). Zigzag scanning has the consequence of improving the chances of consecutive series of zero coefficients, each of which is preceded by a non-zero coefficient. The run/level coding mainly includes replacing each series from the ZZ scanning with a pair of values, one representing the number of successive zero coefficients and the other representing the first following non-zero coefficient.

[0008] At 13, the pairs of values from the RLC are subject to variable length coding (VLC) that includes replacing the more frequent pairs with short codes and replacing the less frequent pairs with long codes, with the aid of correspondence tables defined by the H.261 and MPEG standards. The quantification coefficients can be varied from one block to the next by multiplication by a quantisation coefficient. That quantisation coefficient is inserted during variable length coding in headers preceding the compressed data corresponding to macroblocks.

[0009] Macroblocks of an intra picture are used to compress macroblocks of a subsequent picture of predicted or bidirectional type. Thus, decoding of a predicted or bidirectional picture is likely to be achieved from a previously decoded intra picture. This previously decoded intra picture does not exactly correspond to the actual picture initially received by the compression circuit, since this initial picture is altered by the quantification at 11. Thus, the compression of a predicted or intra picture is carried out from a reconstructed intra picture I1r rather than from the real intra picture I1, so that decoding is carried out under the same conditions as encoding.

[0010] The reconstructed intra picture I1r is stored in a memory area M2 and is obtained by subjecting the macroblocks provided by the quantification 11 to a reverse processing, that is, at 15 an inverse quantification followed at 16 by an inverse DCT.

[0011] FIG. 1B illustrates the compression of a predicted picture P4. The predicted picture P4 is stored in a memory area M1. A previously processed intra picture IIr has been reconstructed in a memory area M2.

[0012] The processing of the macroblocks of the predicted picture P4 is carried out from so-called predictor macroblocks of the reconstructed picture I1r. Each macroblock of picture P4 (reference macroblock) is subject at 17 to motion estimation (generally, the motion estimation is carried out only with the four luminance blocks of the reference macroblocks) . This motion estimation includes searching in a window of picture IIr for a macroblock that is nearest, or most similar to the reference macroblock. The nearest macroblock found in the window is the predictor macroblock. Its position is determined by a motion vector V provided by the motion estimation. The predictor macroblock is subtracted at 18 from the current reference macroblock. The resulting difference macroblock is subjected to the process described with relation to FIG. 1A.

[0013] Like the intra pictures, the predicted pictures serve to compress other predicted pictures and bidirectional pictures. For this purpose, the predicted picture P4 is reconstructed in a memory area M3 by an inverse quantification at 15, inverse DCT at 19, and addition at 19 of the predictor macroblock that was subtracted at 18.

[0014] The vector V provided by the motion estimation 17 is inserted in a header preceding the data provided by the variable length coding of the currently processed macroblock.

[0015] FIG. 1C illustrates the compression of a bidi-

rectional picture B2. Bidirectional pictures are provided for in MPEG standards only. The processing of the bidirectional pictures differs from the processing of predicted pictures in that the motion estimation 17 consists in finding two predictor macroblocks in two pictures I1r and P4r, respectively, that were previously reconstructed in memory areas M2 and M3. Pictures I1r and P4r generally respectively correspond to a picture preceding the bidirectional picture that is currently processed and to a picture following the bidirectional picture.

[0016] At 20, the mean value of the two obtained predictor macroblocks is calculated and is subtracted at 18 from the currently processed macroblock.

[0017] The bidirectional picture is not reconstructed because it is not used to compress another picture.

[0018] The motion estimation 17 provides two vectors V1 and V2 indicating the respective positions of the two predictor macroblocks in pictures I1r and P4r with respect to the reference macroblock of the bidirectional picture. Vectors V1 and V2 are inserted in a header preceding the data provided by the variable length coding of the currently processed macroblock.

[0019] In a predicted picture, an attempt is made to find a predictor macroblock for each reference macroblock. However, in some cases, using the predictor macroblock that is found may provide a smaller compression rate than that obtained by using an unmoved predictor macroblock (zero motion vector), or even smaller than the simple intra processing of the reference macroblock. Thus, depending upon these cases, the reference macroblock is submitted to either predicted processing with the vector that is found, predicted processing with a zero vector, or intra processing.

[0020] In a bidirectional picture, an attempt is made to find two predictor macroblocks for each reference macroblock. For each of the two predictor macroblocks, the process providing the best compression rate is determined, as indicated above with respect to a predicted picture. Thus, depending on the result, the reference macroblock is submitted to either bidirectional processing with the two vectors, predicted processing with only one of the vectors, or intra processing.

[0021] Thus, a predicted picture and a bidirectional picture may contain macroblocks of different types. The type of a macroblock is also data inserted in a header during variable length coding. According to MPEG standards, the motion vectors can be defined with an accuracy of half a pixel. To search a predictor macroblock with a non integer vector, first the predictor macroblock determined by the integer part of this vector is fetched, then this macroblock is submitted to so-called "half-pixel filtering", which includes averaging the macroblock and the same macroblock shifted down and/or to the right by one pixel, depending on the integer or non-integer values of the two components of the vector. According to H.261 standards, the predictor macroblocks may be subjected to low-pass filtering. For this purpose, information is provided with the vector, indicating whether filtering has to be carried out or not.

[0022] The succession of types (intra, predicted, bidirectional) is assigned to the pictures in a predetermined way, in a so-called group of pictures (GOP). A GOP generally begins with an intra picture. It is usual, in a GOP, to have a periodical series, starting from the second picture, including several successive bidirectional pictures, followed by a predicted picture, for example of the form IBBPBBPBB ... where I is an intra picture, B a bidirectional picture, and P a predicted picture. The processing of each bidirectional picture B is carried out from macroblocks of the previous intra or predicted picture and from macroblocks of the next predicted picture.

[0023] The various functional blocks that are used in a typical prior art functional implementation are shown in Figure 2. For clarity, the motion estimation engine and memory for storing macroblocks and video pictures have been omitted.

[0024] In Figure 2, a reference macroblock 200 is supplied to a subtraction circuit 201, where the predictor 202 for that macroblock is subtracted (in the case of B and P pictures, only). The resultant error block (or the original macroblock, for I pictures) is passed on to a DCT block 203, then to a quantisation block 204 for quantisation.

[0025] The quantised macroblock is forwarded to an encoding block 205 and an inverse quantisation block 206. The encoding block 205 takes the quantised macroblock and zig-zag encodes it, performs run level coding on the resultant data, then variable length packs the result, outputting the now encoded bitstream.

[0026] The bitstream is monitored and can be controlled via feedback to a rate control system 207. This controls quantisation (and dequantisation) to meet certain objective for the bitstream. A typical objective is a maximum bit-rate, although other factors can also be used.

[0027] The inverse quantisation block 206 in this Figure is the start of a reconstruction chain that is used to generate a reconstructed version of each frame, so that the frames the motion prediction engine is searching for matching macroblocks are the same as will be regenerated during decoding proper. After inverse quantisation, the macroblock is inverse DCT transformed in IDCT block 208 and added in an adding block 209 to the original predictor used to generate the error macroblock. This reconstructed block is stored in memory for subsequent use in the motion estimation process.

[0028] The various blocks required to generate the encoded output stream have different computational requirements, which themselves can vary according to the particular application or user selected restrictions. Throttling of the output bitstream to meet bandwidth requirements is typically handled by manipulating the quantisation step.

[0029] Pure hardware architectures, while potentially the most efficient, suffer from lack of flexibility since they can support only a restricted range of standards; moreover they have long design/verification cycles. On the

other hand, pure software solutions, while being the most flexible, require high-performance processors unsuited to low-cost consumer applications.

[0030] It would be desirable to provide an architecture that allowed for relatively flexible bitstream control whilst reducing the amount of software=based processing power required.

SUMMARY OF INVENTION

[0031] According to a first aspect of the invention, there is provided compression circuitry for generating an encoded bitstream from a plurality of video frames, the circuitry including:

discrete cosine transform (DCT) circuitry for accepting prediction error macroblocks and generating DCT transformed macroblocks;
a first streaming data connection for streaming the DCT transformed macroblocks from the DCT transformation circuitry to a processor, the processor being configured to run software for:

(i) quantising the DCT transformed macroblocks to generate quantised macroblocks; and
(ii) inverse quantising the quantised macroblocks to generate inverse quantised macroblocks;

a second streaming data connection for streaming the inverse quantised macroblocks from the processor;
inverse discrete cosine transform (IDCT) circuitry for accepting the streamed inverse quantised macroblocks and IDCT transforming them to generate reconstructed prediction error macroblocks;
an addition circuit for adding each reconstructed prediction error macroblock and its corresponding predictor macroblock, thereby to generate a respective reconstructed macroblocks for use in encoding of other macroblocks;
means for zig-zag scanning, run level coding and variable length coding the quantised macroblocks to generate an encoded bitstream.

[0032] Preferably, the DCT and IDCT circuitry perform DCT and IDCT processing at a rate determined by the arrival of data from the relevant data connection.

[0033] Preferably, the first and second streaming data connections are handshake controlled. More preferably, the DCT and IDCT circuitry perform DCT and IDCT processing at a rate determined by the handshake control signals.

[0034] In a preferred form, the processor is configured to run software for implementing the zig-zag scanning and run length coding.

[0035] Preferably, the DCT and IDCT circuitry share hardware. It is particularly preferred that the DCT and IDCT circuitry comprise a single functional block selectively operable in a DCT or IDCT mode.

[0036] In a preferred form, the compression circuitry further includes a motion estimation engine for supplying the predictor macroblocks to the IDCT circuitry. More preferably, the motion estimation engine is configured to generate the prediction error macroblocks by subtracting predictor macroblocks from respective corresponding picture macroblocks of the picture being encoded, and to supply the prediction error macroblocks to the DCT circuitry.

[0037] In a preferred embodiment, the circuitry includes a hardware VLC packer and a third streaming data connection for streaming the run length coded data from the processor to the hardware VLC packer.

[0038] Preferably, the compression circuitry further includes macroblock memory for storing the reconstructed macroblocks.

[0039] It is particularly preferred that the compression circuitry can be configured for decoding of a compressed video stream.

[0040] In a second aspect, the present invention provides a method of generating an encoded bitstream from a plurality of video frames, the method including the steps of:

discrete cosine transforming prediction error macroblocks to generate DCT transformed macroblocks;
streaming the DCT transformed macroblocks from the DCT transformation circuitry to a processor via a first streaming data connection;
in the processor:

(i) quantising the DCT transformed macroblocks to generate quantised macroblocks; and
(ii) inverse quantising the quantised macroblocks to generate inverse quantised macroblocks;

streaming the inverse quantised macroblocks from the processor via a second streaming data connection;
inverse discrete cosine transforming (IDCT) the streamed inverse quantised macroblocks to generate reconstructed prediction error macroblocks;
adding each reconstructed prediction error macroblock and its corresponding predictor macroblock, thereby to generate a respective reconstructed macroblocks for use in encoding of other macroblocks;
zig-zag scanning, run level coding and variable length coding the quantised macroblocks to generate an encoded bitstream.

[0041] Preferably, the DCT and IDCT processing take place at a rate determined by the arrival of data from the relevant data connection.

[0042] Preferably, the first and second streaming data connections are handshake controlled. More preferably, the step of DCT and IDCT processing at a rate determined by the handshake control signals.

[0043] Preferably, the processor is configured to run software for implementing the zig-zag scanning and run length coding.

[0044] In a preferred embodiment, the DCT and IDCT circuitry share hardware. More preferably, the DCT and IDCT circuitry comprise a single functional block selectively operable in a DCT or IDCT mode.

[0045] Preferably, the method further includes the step of receiving, in the IDCT circuitry, the predictor macroblocks from a motion estimation engine. More preferably, the method includes the step, in the motion estimation engine, of generating the prediction error macroblocks by subtracting predictor macroblocks from respective corresponding picture macroblocks of the picture being encoded, and supplying the prediction error macroblocks to the DCT circuitry.

[0046] In a preferred form, the circuitry includes a hardware VLC packer, the method including the step of streaming the run length coded data from the processor to the hardware VLC packer via a third streaming data connection.

[0047] Preferably, the reconstructed macroblocks are stored in macroblock memory.

[0048] In each aspect of the invention, it is preferred that the encoded bitstream conforms to MPEG, MPEG-2 and/or H.261 standards.

BRIEF DESCRIPTION OF DRAWINGS

[0049]

Figures 1A to 1C, described above, illustrate three picture compression processes according to H.261 and MPEG standards;

Figure 2, described above, is a simplified schematic of the functional blocks in a typical MPEG encoding scheme, in accordance with the prior art;

Figure 3 is a schematic of an encoder loop, in accordance with the invention;

Figure 4 is a schematic of compression circuitry for generating an encoded bitstream from a plurality of video frames, in accordance with the invention, in encoding mode;

DETAILED DESCRIPTION

[0050] Figure 3 shows an overview of the functional blocks of the preferred form of the invention, in which hardware functionality is represented by rectangular blocks and software functionality is represented by an oval block.

[0051] The functional blocks include an subtraction circuit 300 for subtracting each predictor macroblock, as supplied by the motion estimation engine (described later) from its corresponding picture macroblock, to generate a prediction error macroblock. For an I picture, there is no predictor, so the macroblock is passed through the subtraction circuit with no change.

[0052] The prediction error macroblock is supplied to a DCT circuit 301 where a forward discrete cosine transform is performed. Such hardware and its operation are well known in the prior art and so have not been described here in further detail.

[0053] The output of the DCT is streamed to a processor 302 (described later) which performs the quantisation, zig-zag coding, a run level coding steps in the encoding process. The resultant data is variable length coded and output as an encoded bitstream. In the simplified schematic of Figure 3, the variable length coding takes place in software. However, in an alternative embodiment described later, the variable length coding and packing, or just packing, is performed in hardware, since this provides a drastic increase in performance compared to software coding running on a general purpose processor.

[0054] As well as these steps, the processor also performs inverse quantisation, and the resultant inverse quantised macroblocks are sent to an inverse DCT (IDCT) circuit 303 via a streaming interface. An inverse DCT is performed and the resultant reconstructed error macroblock is added to the original predictor macroblock (for P and B pictures only) by an addition circuit 304. The predictor macroblocks have been delayed in a delay buffer 305. For I and P pictures, the macroblock is fully reconstructed after the IDCT circuit. The resultant reconstructed macroblocks are then stored in memory (not shown) for use by the motion estimation engine in generating predictors for future macroblocks. This is necessary because it is reconstructed macroblocks that a decoder will subsequently use to reconstruct the pictures.

[0055] Turning to Figure 4, there is shown a more detailed version of the schematic of Figure 3, and like features are denoted by corresponding reference numerals. In Figure 4, the motion estimation engine 400 for use with the encoding circuitry is also shown. The motion estimation engine 400 determines the best matching macroblock (or average of two macroblocks) for each macroblock in the frame (for B and P pictures only) and subtracts it from the macroblock being considered to generate a predictor error macroblock. The method of selecting predictor macroblocks does not form part of the present invention and so is not described in greater detail herein.

[0056] The motion estimation engine 400 outputs the macroblocks, associated predictor macroblocks and vectors, and other information such as frame type and encoding modes, to DCT/IDCT circuitry via a direct link. Alternatively, this information can be transferred over a

data bus. Data bus transfer principles are well known and so is not described in detail.

[0057] The DCT and IDCT steps are performed in a DCT/IDCT block 401, which includes combined DCT/IDCT circuitry 301/303 that is selectable to perform either operation on incoming data. The input is selected by way of a multiplexer 402, the operation of which will be described in greater detail below. The output of the multiplexer is supplied to the delay block 305 and the DCT/IDCT circuitry 301/303. Additional data supplied by the motion estimation engine 400, such as the motion vector(s), encoding decisions (intra/non-intra, MC/no MC, field/frame prediction, field/frame DCT) is routed past the delay and DCT/IDCT blocks to a first streaming data interface SDI 403.

[0058] The outputs of the delay block and the DCT/IDCT circuitry are supplied to an addition circuit 304, the output of which is sent to memory 450. The output of the DCT/IDCT block 301/303 is also supplied to the first SDI port 403.

[0059] The first SDI port 403 accepts data from the DCT/IDCT block 301/303 and the multiplexer 402 and converts it into a format suitable for streaming transmission to a corresponding second streaming SDI port 404. The streaming is controlled by a handshake arrangement between the respective SDI ports. The second streaming SDI port 404 takes the streaming data from the first SDI port 403 and converts it back into a format suitable for use within the processor 302.

[0060] Once the data has been transformed back into a synchronous format, the processor performs quantisation 405, inverse quantisation 406 and zig-zag/run level coding 407 as described previously. It will be appreciated that the particular implementations of these steps in software is now relevant to the present invention, and so is not described in detail.

[0061] After inverse quantisation, the macroblock is returned to a third SDI port 408, which operates in the same way as the first streaming port to convert and stream the data to a fourth SDI port 409, which converts the data for synchronous use and supplies it to the multiplexer 402.

[0062] The processor 302 outputs the run level coded data to a fifth SDI port 410, which in a similar fashion to the first and third SDI ports, formats the data for streaming transmission to a sixth SDI port 411, which in turn reformats the data into a synchronous format. The data is then variable length coded and packed in hardware VLC circuitry 412. The particular workings of the hardware VLC packing circuitry 412 are well known in the art, are not critical to the present invention and so will not be described in detail. Indeed, as mentioned previously, the VLC operation can be performed in software by the processor, for a corresponding cost in processor cycles.

[0063] It will be appreciated that a number of control lines and ancillary detail has been omitted for clarity. For example, it is clear the multiplexer and DCT/IDCT block 301/303 need to be controlled to ensure that the correct data is being fed to the DCT/IDCT block and that the correct operation is being performed. For example, when the initial DCT operation 301 is being performed, the multiplexer 402 is controlled to provide data from the bus (supplied by the motion estimation engine) to the DCT/IDCT block 301/303, which is set to DCT mode. However, when performing the IDCT operation 303, the multiplexer 402 sends data from the fourth SDI port 409 to the DCT/IDCT block 301/303, which is set to IDCT mode.

[0064] Similarly, some support hardware that would exist in the actual implementation has been omitted. An obvious example is buffers on the various inputs and output. It would be usual in such circuitry to include FIFO buffers supporting the SDI ports to maximise throughput. For the purposes of clarity, such support hardware is not explicitly shown. However, it will be understood by those skilled in the art to be implicitly present in any practical application of the invention.

[0065] It will be appreciated that, in the encoding mode described above, the DCT and IDCT functions of the DCT/IDCT block 301/303 will be performed in an interleaved manner, with one or more DCT operations being interleaved with one or more IDCT operations, depending upon the order of I, P and B pictures being encoded.

[0066] With slight modifications to control software and circuitry, the encoding circuitry described above can perform decoding of an encoded MPEG stream. This is because the inverse quantisation software and IDCT hardware are common to the encoding and decoding process. There are at least three ways this can be achieved:

1. If it is only required to offload the IDCT processing from the processor, the dequantised coefficient blocks can be streamed from the processor to the IDCT/DCT block 301/303 via the third and fourth SDI ports 408 and 409. The results of the IDCT are then read back via the first and second SDI ports 403 and 404.

2. Option 1 can be extended to allow more of the decoding load to be passed to the DCT/IDCT block 401. In particular, the predictor blocks are read into the delay buffer 305. The coefficient blocks are then read in via the same route by the DCT/IDCT block 301/303 (in IDCT mode). After the IDCT has taken place, the predictor and IDCT processed macroblocks are combined by the addition circuitry 304 and written to system memory via the system data bus.

3. In an alternative to second decoding arrangement, the motion estimation block is configured to provide the predictor blocks to the delay buffer 305 via the multiplexer 402. The coefficient blocks are provided to the DCT/IDCT block 301/303 (in IDCT

mode), and the remainder of the procedure is as per the second decoding arrangement.

[0067] Although the invention has been described with reference to a number of specific examples, it will be appreciated by those skilled in the art that the invention can be embodied in many other forms.

Claims

1. Compression circuitry for generating an encoded bitstream from a plurality of video frames, the circuitry including:

   discrete cosine transform (DCT) circuitry for accepting prediction error macroblocks and generating DCT transformed macroblocks;
   a first streaming data connection for streaming the DCT transformed macroblocks from the DCT transformation circuitry to a processor, the processor being configured to run software for:

   (i) quantising the DCT transformed macroblocks to generate quantised macroblocks; and
   (ii) inverse quantising the quantised macroblocks to generate inverse quantised macroblocks;

   a second streaming data connection for streaming the inverse quantised macroblocks from the processor;
   inverse discrete cosine transform (IDCT) circuitry for accepting the streamed inverse quantised macroblocks and IDCT transforming them to generate reconstructed prediction error macroblocks;
   an addition circuit for adding each reconstructed prediction error macroblock and its corresponding predictor macroblock, thereby to generate a respective reconstructed macroblocks for use in encoding of other macroblocks;
   means for zig-zag scanning, run level coding and variable length coding the quantised macroblocks to generate an encoded bitstream.

2. Compression circuitry according to claim 1, wherein the DCT and IDCT circuitry perform DCT and IDCT processing at a rate determined by the arrival of data from the relevant data connection.

3. Compression circuitry according to claim 1 or 2, wherein the first and second streaming data connections are handshake controlled.

4. Compression circuitry according to claim 3, wherein the DCT and IDCT circuitry perform DCT and IDCT processing at a rate determined by the handshake control signals.

5. Compression circuitry according to any one of the preceding claims, wherein the processor is configured to run software for implementing the zig-zag scanning and run length coding.

6. Compression circuitry according to any one of the preceding claims, wherein the DCT and IDCT circuitry share hardware.

7. Compression circuitry according to claim 6, wherein the DCT and IDCT circuitry comprise a single functional block selectively operable in a DCT or IDCT mode.

8. Compression circuitry according to any one of the preceding claims, further including a motion estimation engine for supplying the predictor macroblocks to the IDCT circuitry.

9. Compression circuitry according to claim 8, wherein the motion estimation engine is configured to generate the prediction error macroblocks by subtracting predictor macroblocks from respective corresponding picture macroblocks of the picture being encoded, and to supply the prediction error macroblocks to the DCT circuitry.

10. Compression circuitry according to any one of the preceding claims, wherein the circuitry includes a hardware VLC packer and a third streaming data connection for streaming the run length coded data from the processor to the hardware VLC packer.

11. Compression circuitry according to any one of the preceding claims, further including macroblock memory for storing the reconstructed macroblocks.

12. Compression circuitry according to any one of the preceding claims, configured for decoding of a compressed video stream.

13. Compression circuitry according to any one of the preceding claims, configured to generate an encoded bitstream in accordance with MPEG, MPEG-2 and/or H.261 standards.

14. A method of generating an encoded bitstream from a plurality of video frames, the method including the steps of:

   discrete cosine transforming prediction error macroblocks to generate DCT transformed macroblocks;
   streaming the DCT transformed macroblocks from the DCT transformation circuitry to a proc-

essor via a first streaming data connection;
in the processor:

(i) quantising the DCT transformed macroblocks to generate quantised macroblocks; and
(ii) inverse quantising the quantised macroblocks to generate inverse quantised macroblocks;

streaming the inverse quantised macroblocks from the processor via a second streaming data connection;
inverse discrete cosine transforming (IDCT) the streamed inverse quantised macroblocks to generate reconstructed prediction error macroblocks;
adding each reconstructed prediction error macroblock and its corresponding predictor macroblock, thereby to generate a respective reconstructed macroblocks for use in encoding of other macroblocks;
zig-zag scanning, run level coding and variable length coding the quantised macroblocks to generate an encoded bitstream.

15. A method according to claim 14, wherein the DCT and IDCT processing take place at a rate determined by the arrival of data from the relevant data connection.

16. A method according to claim 14 or 15, wherein the first and second streaming data connections are handshake controlled.

17. A method according to claim 16, including the step of DCT and IDCT processing at a rate determined by the handshake control signals.

18. A method according to any one of claims 14 to 17, wherein the processor is configured to run software for implementing the zig-zag scanning and run length coding.

19. A method according to any one of claims 14 to 18, wherein the DCT and IDCT circuitry share hardware.

20. A method according to claim 19, wherein the DCT and IDCT circuitry comprise a single functional block selectively operable in a DCT or IDCT mode.

21. A method according to any one of claims 14 to 20, further including the step of receiving, in the IDCT circuitry, the predictor macroblocks from a motion estimation engine.

22. A method according to claim 21, including the step, in the motion estimation engine, of generating the prediction error macroblocks by subtracting predictor macroblocks from respective corresponding picture macroblocks of the picture being encoded, and supplying the prediction error macroblocks to the DCT circuitry.

23. A method according to any one of claim 14 to 22, wherein the circuitry includes a hardware VLC packer, the method including the step of streaming the run length coded data from the processor to the hardware VLC packer via a third streaming data connection.

24. A method according to any one of claims 14 to 23, wherein the reconstructed macroblocks are stored in macroblock memory.

25. A method according to any one of claims 14 to 24, wherein the encoded bitstream conforms to MPEG, MPEG-2 and/or H.261 standards.

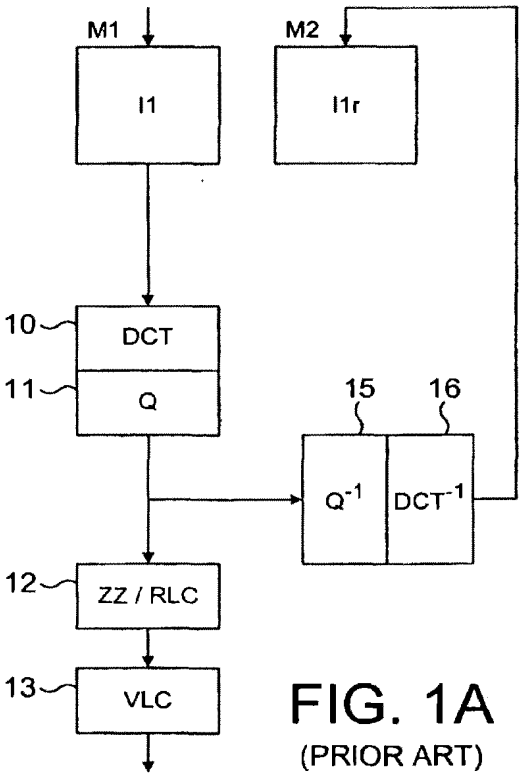


FIG. 1A
(PRIOR ART)

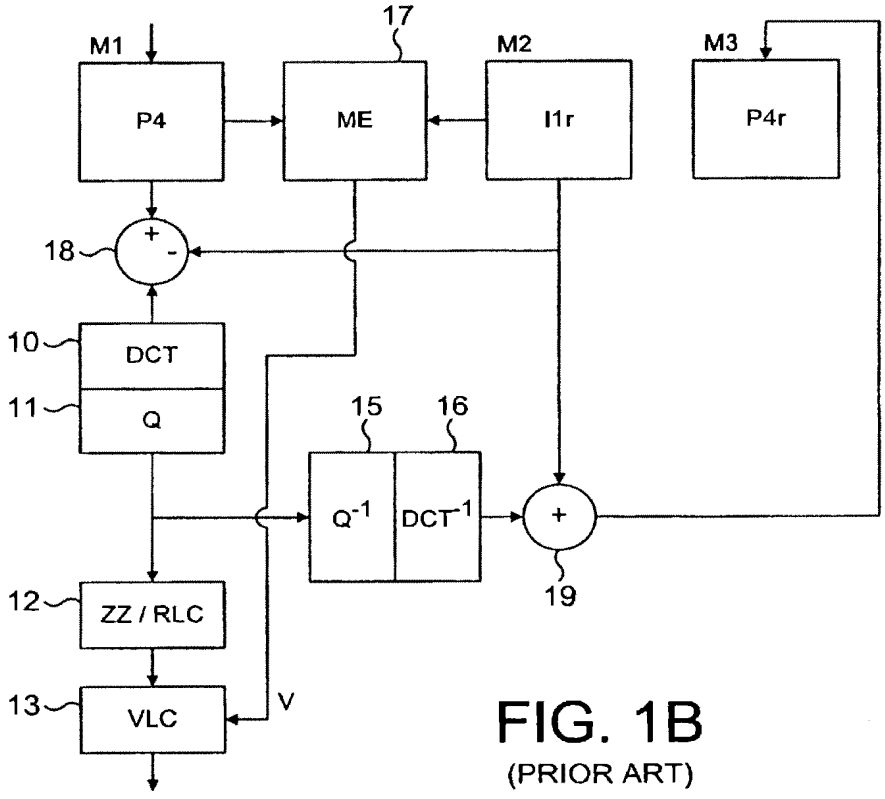


FIG. 1B
(PRIOR ART)

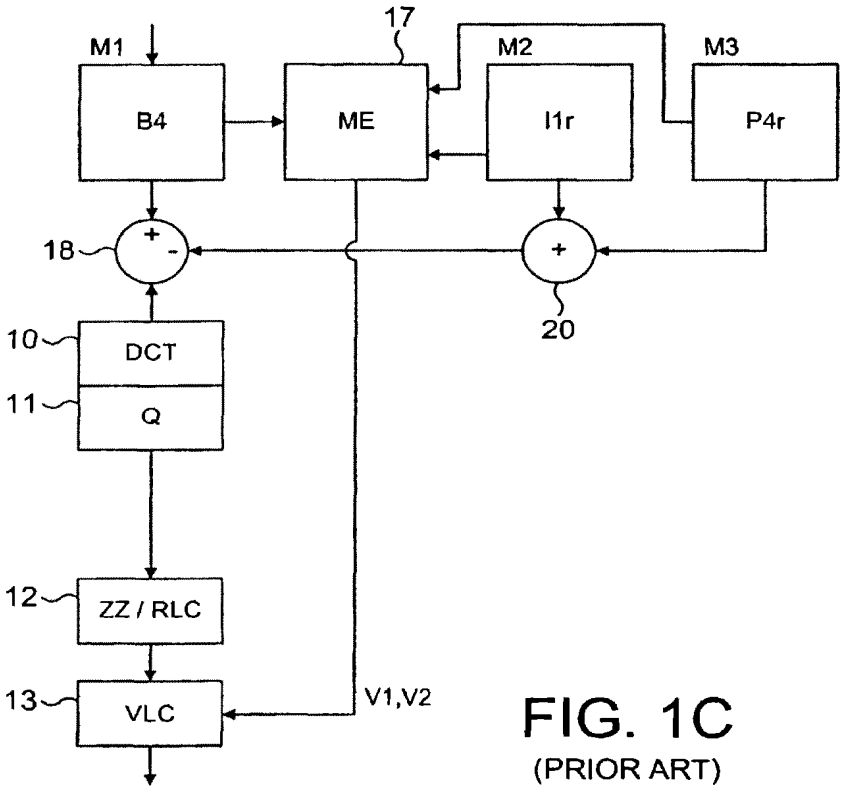


FIG. 1C
(PRIOR ART)

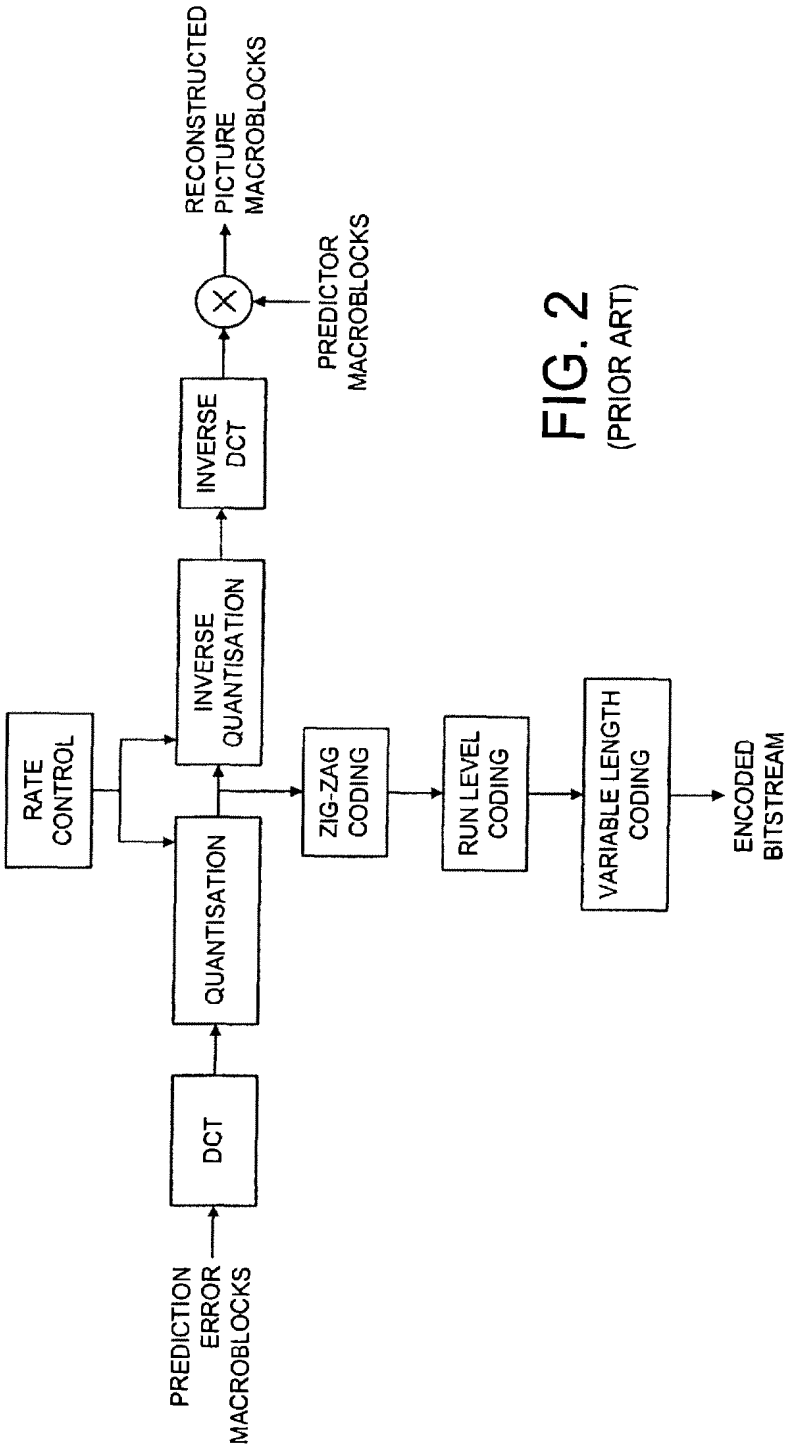


FIG. 2
(PRIOR ART)

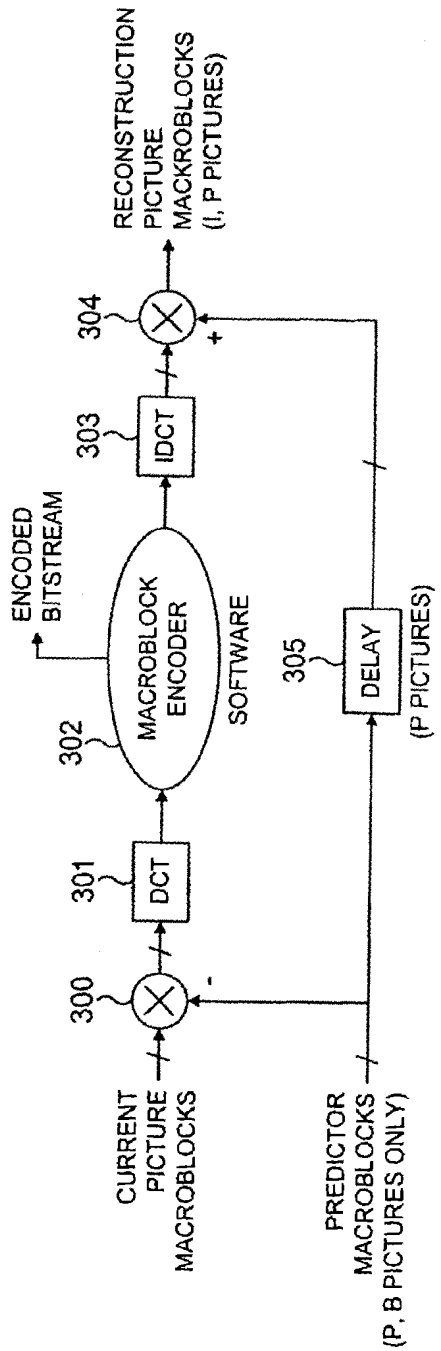
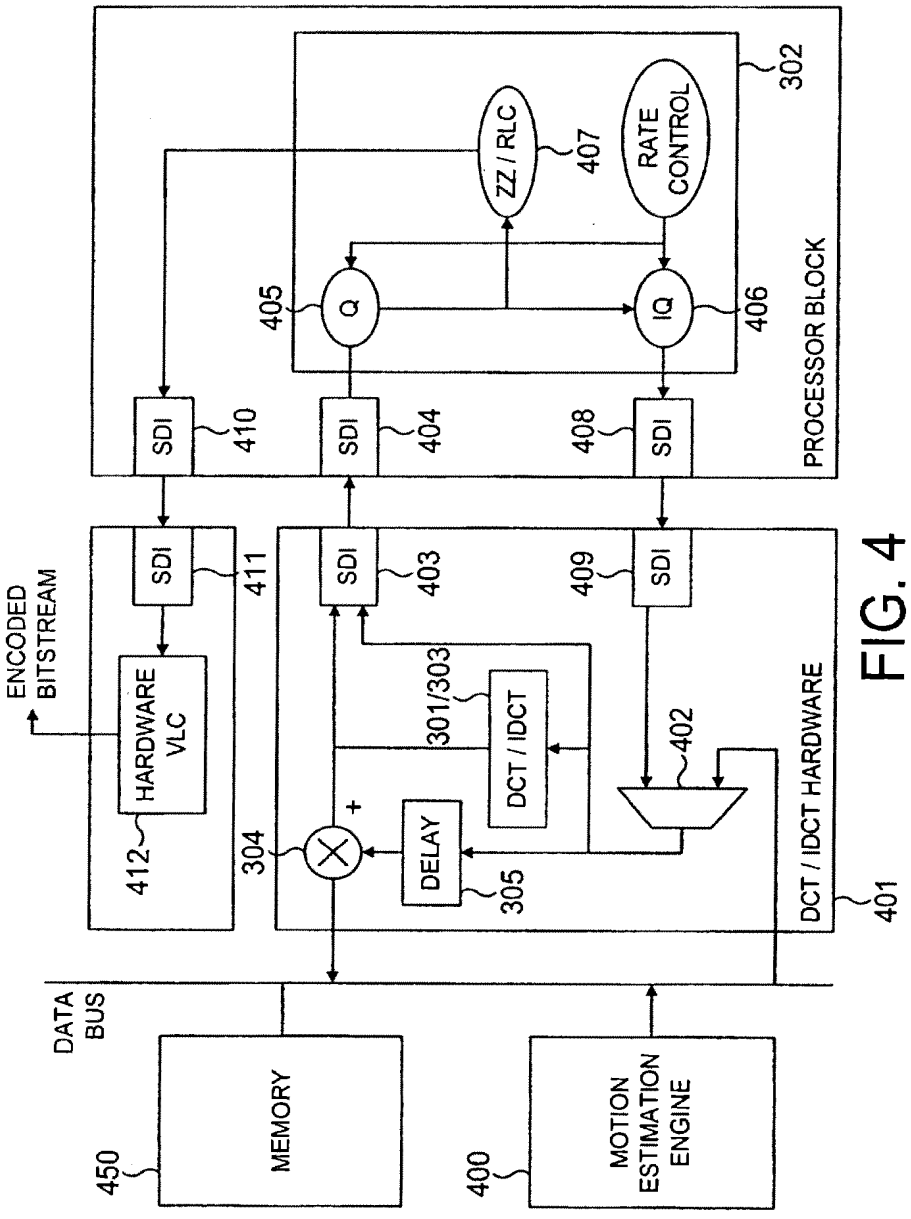

CURRENT PICTURE MACROBLOCKS
PREDICTOR MACROBLOCKS (P, B PICTURES ONLY)
300
301
DCT
302
MACROBLOCK ENCODER
SOFTWARE
ENCODED BITSTREAM
303
IDCT
304
RECONSTRUCTION PICTURE MACKROBLOCKS (I, P PICTURES)
305
DELAY
(P PICTURES)
-
+

FIG. 3


ENCODED BITSTREAM
HARDWARE VLC
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SDI
411
SDI
410
SDI
404
SDI
403
SDI
409
SDI
408
SDI
405
Q
ZZ / RLC
407
RATE CONTROL
IQ
406
302
PROCESSOR BLOCK
301/303
DCT / IDCT
402
304
+
DELAY
305
DCT / IDCT HARDWARE
401
DATA BUS
450
MEMORY
400
MOTION ESTIMATION ENGINE

FIG. 4

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 02 25 1932

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 6 091 857 A (SHAW STEVEN M ET AL) 18 July 2000 (2000-07-18) * column 18, line 29 - line 44 * * column 20, line 22 - column 21, line 24 * * column 27, line 38 - column 28, line 60 * * column 29, line 19 - line 30 * * figures 8,12 *	1-25	H04N7/50
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TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H04N

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	17 September 2002	Lombardi, G

CATEGORY OF CITED DOCUMENTS

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